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# Study on Advanced Modular Cascaded Linear Amplifier with Unequal Capacitor Voltages of H-bridge Cells

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This paper proposes a new topology of modular cascaded linear amplifier which the circuit consists of multiple H-bridges and a dc input voltage source. The proposed amplifier is operated as an inductorless inverter with a very low noise. The proposed amplifier can balance the capacitor voltage of each cell. Moreover, the capacitor voltages are controlled to be unequal to increase the voltage level, resulting in the increase of the theoretical maximum efficiency. A simulation result is provided to verify the proper operation of the proposed amplifier.

Keywords: cascaded H-bridge, inverter, linear amplifier, multilevel converter

## 1. Introduction

The switched mode power converter is commonly used for power conversion because of its high conversion efficiency. However, its high switching frequency causes a large noise. On the other hand, the linear power amplifier is capable to perform the power conversion with a very low noise. But its conversion efficiency is typically low which is lower than 80%. Some attempts have been reported to integrate the concepts of switched mode power converter and the linear power amplifier aiming to reduce the noise and improve the efficiency at the same time [1]–[5].

The major power loss in the linear power amplifiers comes from the applied voltage and current to the MOSFETs operated at the linear region. In this paper, The MOSFETs which are operated at the linear region are simply called as the active-state MOSFETs. The switching operation produce a multilevel voltage source which the voltage follows the output voltage. The difference between the generated multilevel voltage and the output voltage is the voltage across the active-state MOSFETs. The voltage of the active-state MOSFETs is reduced by increasing the number of voltage level; thus, the conversion efficiency can be improved.

Various multilevel techniques such as diode-clamped [1, 2], modular-cascaded-converter [3], and flying-capacitor [4] have been combined with the operation of the linear power amplifier [5]. The diode clamped linear amplifier (DCLA) requires multiple dc input voltage sources [1] or a dc-voltage balancing circuit [2], and the modular cascaded converter requires an isolated single input to multi output dc-to-dc power converter [3]. This additional power conversion stage might produce a significant power loss and become impractical especially when the number of level is high.

A capacitor voltage balancing control was proposed for the flying capacitor linear amplifier (FCLA) in [4]. The voltage balancing control makes it possible to operate the FCLA with two dc input voltage sources only. This paper applied similar voltage balancing control to the proposed topology of modular cascaded linear amplifier (MCLA). Moreover, the capacitor voltages were controlled to be unequal to increase the number of voltage level, resulting in the increase of the theoretical efficiency. A simulation result is provided to verify the operation of voltage balancing and the theoretical efficiency.

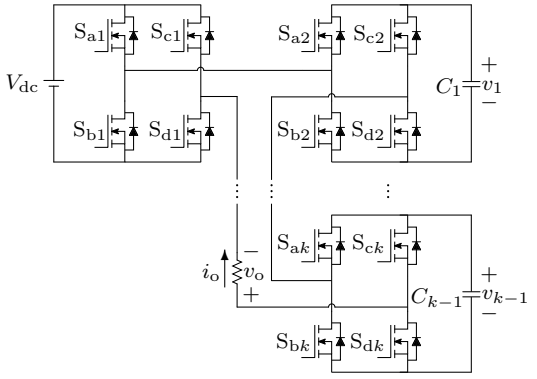


Fig. 1. Modular cascaded linear amplifier consisting of $k$ H-bridge circuits.

## 2. Modular Cascaded Linear Amplifier

Fig. 1 shows the proposed topology of modular cascaded linear amplifier (MCLA) which the circuit consists of $k$ H-bridge circuits. The first H-bridge circuit is the main H-bridge. The dc input voltage source is connected to the dc side of the main H-bridge. Other H-bridge circuits are the H-bridge cells, whose dc sides are connected to the capacitors.

The main H-bridge can be modeled as a three level voltage source $v_{\rm i} = \{V_{\rm dc}, 0, -V_{\rm dc}\}$ as shown in Fig. 2. If the capacitor voltage of the $m$-th H-bridge circuit $v_{m-1}$ has a constant dc value and a negligible ripple, then this H-bridge cell can also be modeled as a three level voltage source $v_{{\rm C}m-1} = \{v_{m-1}, 0, -v_{{\rm m}-1}\}$ as shown in Fig. 3.

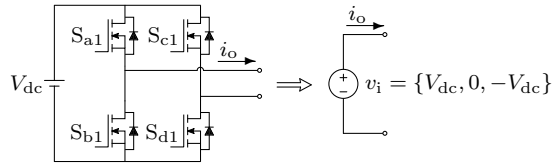


Fig. 2. Equivalent circuit of the main H-bridge circuit.

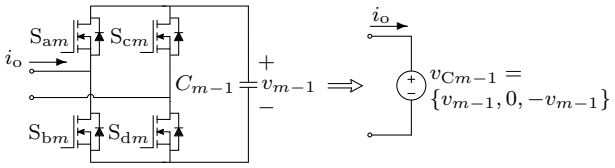


Fig. 3. Equivalent circuit of the $m$-th H-bridge circuit.

The usage of H-bridge circuits makes it possible to implement the MCLA for various applications; however, this paper discusses only the implementation of the MCLA as an inverter with sinusoidal output and pure resistive load. Tables I and II show the used switching modes of the main H-bridge and $m$-th H-bridge circuits. "on", "off", and "act." are the on, off, and active states of the MOSFET, and "fwd" indicates the forward conduction of the body diode. In the active state, the MOSFETs is operated at the linear region. Each MOSFET in the on-state can be operated in the active state. The active-state MOSFET regulates the output voltage in the noiseless manner. And more than one MOSFETs can be operated in the active state at the same time to distribute the ohmic loss.

The charging state of the capacitor $C_{m-1}$ is shown in Table II. $C_{m-1}$ is charged and discharged when $v_{Cm-1} = v_{m-1}$ and $-v_{m-1}$ at $i_o \geq 0$. The charging state is reversed at $i_o < 0$ where $C_{m-1}$ is discharged and charged when $v_{Cm-1} = v_{m-1}$ and $-v_{m-1}$, respectively.

TABLE I
SWITCHING MODES OF THE MAIN H-BRIDGE CIRCUIT

| $i_o$ | $S_{a1}$ | $S_{b1}$ | $S_{c1}$ | $S_{d1}$ | $v_i$ |
|---|---|---|---|---|---|
| $i_o \geq 0$ | on or act. | off | off | on or act. | $V_{dc}$ |
| | off | fwd | off | on | 0 |
| $i_o < 0$ | off | on or act. | off | fwd | 0 |
| | off | on or act | on or act. | off | $-V_{dc}$ |

TABLE II
SWITCHING MODES OF THE $m$-TH H-BRIDGE CIRCUIT

| $i_o$ | $S_{am}$ | $S_{bm}$ | $S_{cm}$ | $S_{dm}$ | $v_{Cm-1}$ | $C_{m-1}$ |
|---|---|---|---|---|---|---|
| $i_o \geq 0$ | fwd | off | off | fwd | $v_{m-1}$ | charge |
| | off | on or act. | off | fwd | 0 | - |
| | off | on or act. | on or act. | off | $-v_{m-1}$ | discharge |
| $i_o < 0$ | on or act. | off | off | on or act. | $v_{m-1}$ | discharge |
| | off | fwd | off | on or act. | 0 | - |
| | off | fwd | fwd | off | $-v_{m-1}$ | charge |

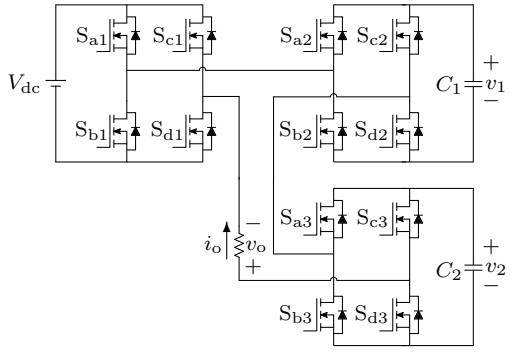


Fig. 4. Modular cascaded linear amplifier consisting of three H-bridge circuits.

## 3. MCLA with Equal Capacitor Voltages

The MCLA with one dc input voltage source is capable to achieve capacitor voltage balancing similar to the FCLA with two dc input voltage sources [4]. If all capacitor voltages are set to be equal to $V_{dc}/k$, then the reqired number of MOSFETs and capacitors are identical to the FCLA. The differences between the FCLA and MCLA are only the rated voltages of the capacitors and MOSFETs. The FCLA requires high rated voltages of the capacitors, whereas the MOSFETs in the main H-bridge circuit of the MCLA must withstand the drain-to-source voltage of $V_{dc}$.

Considering the similarities between the MCLA and FCLA, the operation of the MCLA with equal capacitor voltages is defined as the basic operation. This basic operation is explained by using the MCLA with three H-bridge circuits ($k = 3$) as shown in Fig. 4. The voltage balancing is achieved at $v_1 = v_2 = V_{dc}/3$. Table III shows the list of used switching modes to achieve voltage balancing for the basic operation. Since all capacitor voltages equal $V_{dc}/3$, there are three ranges of the output voltage reference $v_o^*$ at each direction of $i_o$. Only one switching mode is used at $2V_{dc}/3 \leq v_o^* < V_{dc}$ and $-V_{/rmdc} < v_o^* \leq -2V_{dc}/3$ because the capacitors $C_1$ and $C_2$ are neither charged nor discharged in these ranges. Other ranges use sequences of switching modes to achieve voltage balancing.

Fig. 5 shows the mode transition diagram for voltage balancing. The transition diagrams at $i_o \geq 0$ and $i_o < 0$ are identical; thus, they are illustrated in the same figure where the switching modes and transition events inside bracket belong to the transition diagram at $i_o < 0$. The voltage balancing can be achieved at each voltage range by feeding the actual capacitor voltage $v_1$ and $v_2$ to the controller. The controller changes the switching modes according to $v_1$ and $v_2$ and maintains them in a range of $V_{dc}/3 \leq \{v_1, v_2\} \leq V_{dc}/3 + V_r$, where $V_r$ is the amplitude of the capacitor ripple voltage. The value of $V_r$ is set in the controller.

## 4. MCLA with Unequal Capacitor Voltages

### ⟨4.1⟩ Operating Principle

This paper proposes to operate the MCLA with unequal capacitor voltages. This proposal is applicable for the MCLA

TABLE III
SWITCHING MODES OF MCLA CONSISTING OF THREE H-BRIDGE CIRCUITS WITH EQUAL CAPACITOR VOLTAGES

| $i_o$ | $v_o^*$ | Mode | $v_i$ | $v_{C1}$ | $v_{C2}$ | $C_1$ | $C_2$ |
|---|---|---|---|---|---|---|---|
| $i_o \geq 0$ | $\frac{2}{3}V_{dc} \leq v_o^* < V_{dc}$ | p | $V_{dc}$ | 0 | 0 | - | - |
| | $\frac{1}{3}V_{dc} \leq v_o^* < \frac{2}{3}V_{dc}$ | p1c | $V_{dc}$ | $v_1$ | 0 | charge | - |
| | | p2c | $V_{dc}$ | 0 | $v_2$ | - | charge |
| | | p3dd | 0 | $-v_1$ | $-v_2$ | discharge | discharge |
| | $0 \leq v_o^* < \frac{1}{3}V_{dc}$ | p3cc | $V_{dc}$ | $v_1$ | $v_2$ | charge | charge |
| | | p1d | 0 | $-v_1$ | 0 | discharge | - |
| | | p2d | 0 | 0 | $-v_2$ | - | discharge |
| $i_o < 0$ | $-\frac{1}{3}V_{dc} < v_o^* \leq 0$ | n3cc | $-V_{dc}$ | $-v_1$ | $-v_2$ | charge | charge |
| | | n1d | 0 | $v_1$ | 0 | discharge | - |
| | | n2d | 0 | 0 | $v_2$ | - | discharge |
| | $-\frac{2}{3}V_{dc} < v_o^* \leq -\frac{1}{3}V_{dc}$ | n1c | $-V_{dc}$ | $-v_1$ | 0 | charge | - |
| | | n2c | $-V_{dc}$ | 0 | $-v_2$ | - | charge |
| | | n3dd | 0 | $v_1$ | $v_2$ | discharge | discharge |
| | $-V_{dc} < v_o^* \leq -\frac{2}{3}V_{dc}$ | n | $-V_{dc}$ | 0 | 0 | - | - |

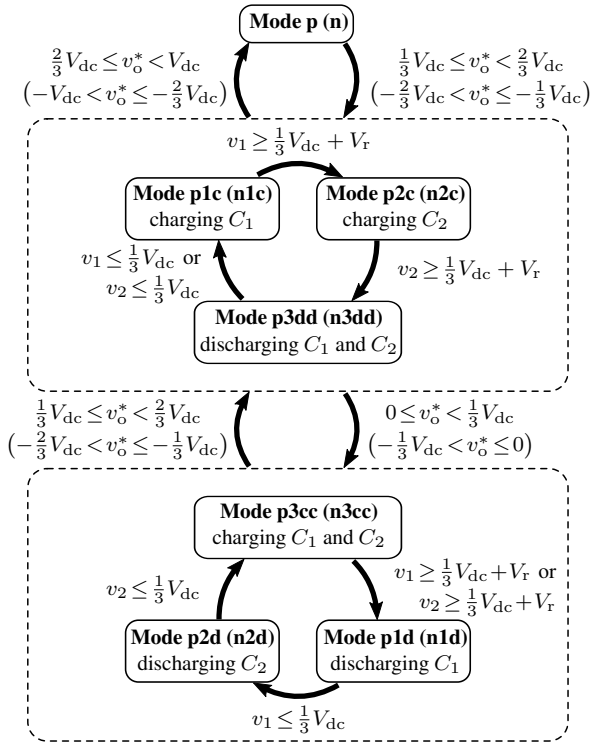


Fig. 5. Mode transition diagram for voltage balancing at $v_{C1} = v_{C2} = V_{dc}/3$.

which the circuit consist of at least three H-bridges. The proposed capacitor voltage of the $m$-th H-bridge circuit is given by

$$v_{m-1} = \frac{m-1}{\left(\sum_{j=1}^{k-1} j\right) + 1} V_{dc}. \quad (1)$$

The MCLA with unequal capacitor voltages generates a multilevel voltage which the step voltage is equal to $v_1$. This

TABLE IV
SWITCHING MODES OF MCLA CONSISTING OF THREE H-BRIDGE CIRCUITS WITH UNEQUAL CAPACITOR VOLTAGES

| $i_o$ | $v_o^*$ | Mode | $v_i$ | $v_{c1}$ | $v_{c2}$ | $C_1$ | $C_2$ |
|---|---|---|---|---|---|---|---|
| $i_o \geq 0$ | $\frac{3}{4}V_{dc} \leq v_o^* < V_{dc}$ | p | $V_{dc}$ | 0 | 0 | - | - |
| | $\frac{1}{2}V_{dc} \leq v_o^* < \frac{3}{4}V_{dc}$ | p1c | $V_{dc}$ | $v_1$ | 0 | charge | - |
| | | p3dc | $V_{dc}$ | $-v_1$ | $v_2$ | discharge | charge |
| | | p3dd | 0 | $-v_1$ | $-v_2$ | discharge | discharge |
| | $\frac{1}{4}V_{dc} \leq v_o^* < \frac{1}{2}V_{dc}$ | p2c | $V_{dc}$ | 0 | $v_2$ | - | charge |
| | | p2d | 0 | 0 | $-v_2$ | - | discharge |
| | $0 \leq v_o^* < \frac{1}{4}V_{dc}$ | p3cc | $V_{dc}$ | $v_1$ | $v_2$ | charge | charge |
| | | p1d | 0 | $-v_1$ | 0 | discharge | - |
| | | p3cd | 0 | $v_1$ | $-v_2$ | charge | discharge |
| $i_o < 0$ | $-\frac{1}{4}V_{dc} < v_o^* \leq 0$ | n3cc | $-V_{dc}$ | $-v_1$ | $-v_2$ | charge | charge |
| | | n1d | 0 | $v_1$ | 0 | discharge | - |
| | | n3cd | 0 | $-v_1$ | $v_2$ | charge | discharge |
| | $-\frac{1}{2}V_{dc} < v_o^* \leq -\frac{1}{4}V_{dc}$ | n2c | $-V_{dc}$ | 0 | $-v_2$ | - | charge |
| | | n2d | 0 | 0 | $v_2$ | - | discharge |
| | $-\frac{3}{4}V_{dc} < v_o^* \leq -\frac{1}{2}V_{dc}$ | n1c | $-V_{dc}$ | $-v_1$ | 0 | charge | - |
| | | n3dc | $-V_{dc}$ | $v_1$ | $-v_2$ | discharge | charge |
| | | n3dd | 0 | $v_1$ | $v_2$ | discharge | discharge |
| | $-V_{dc} < v_o^* \leq -\frac{3}{4}V_{dc}$ | n | $-V_{dc}$ | 0 | 0 | - | - |

step voltage is lower than the step voltage of the MCLA with equal capacitor voltages.

Table IV shows the used switching modes of the three H-bridge MCLA to achieve voltage balancing at the unequal capacitor voltages of $v_1 = V_{dc}/4$ and $v_2 = V_{dc}/2$. Since the step voltage is equal to $v_1 = V_{dc}/4$, there are eight ranges of $v_o^*$ . The capacitors are neither charged nor discharged at the highest and lowest ranges of $v_o^*$; thus only one switching mode is used at these ranges similar to the operation of the MCLA with equal capacitor voltages. Fig. 6 shows the mode transition diagram to achieve voltage balancing. $C_2$ can be solely charged and discharged at $V_{dc}/4 \leq v_o^* < V_{dc}/2$ and $-V_{dc}/4 < v_o^* \leq -V_{dc}/2$; thus, only $v_2$ is regulated at these ranges. At $V_{dc}/2 \leq v_o^* < 3V_{dc}/4$ and $-3V_{dc}/4 < v_o^* \leq -V_{dc}/2$, the charging mode of $C_1$ is used twice in every cycle to realize voltage balancing. A similar voltage balancing sequence is also used at $0 \leq v_o^* < 1V_{dc}/4$ and $-V_{dc}/4 < v_o^* \leq 0$ where the discharging mode of $C_1$ is used twice in every cycle.

### ⟨4.2⟩ Evaluation of MCLA with Unequal Capacitor Voltages

The theoretical conversion efficiency of MCLA with equal capacitor voltages is given by

$$\eta = \frac{\pi k^2}{2\sum_{j=1}^{k} \sqrt{8kj - 4j^2}}, \quad (2)$$

where it is assumed that:

1) The on-resistance of the MOSFETs and forward voltage of the body diode are zero,

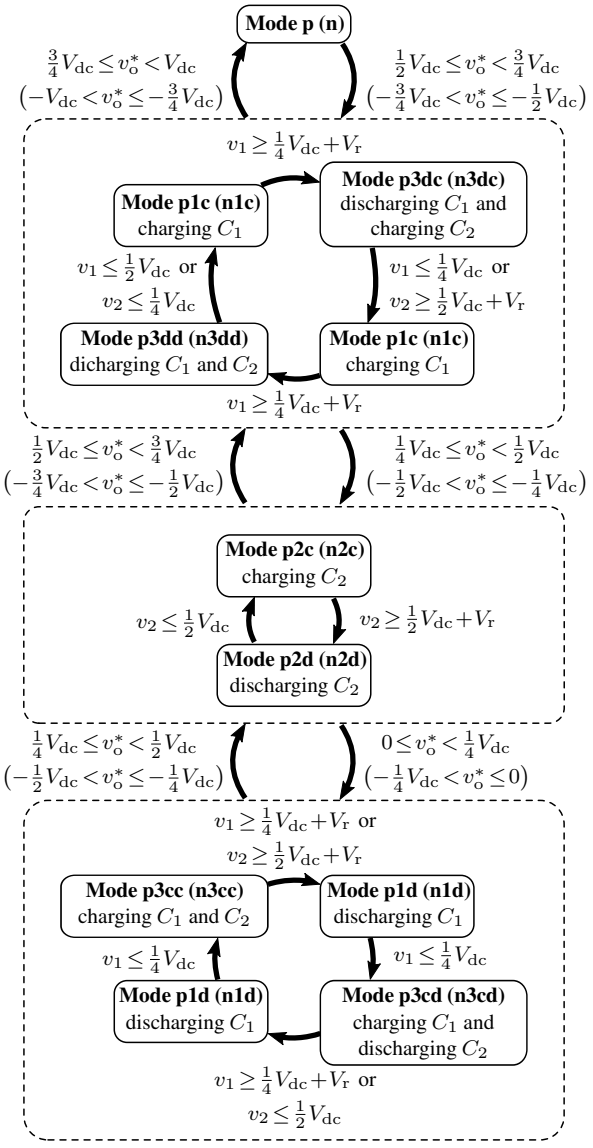


Fig. 6. Mode transition diagram of MCLA for voltage balancing at $v_1 = V_{\rm dc}/4$ and $v_2 = V_{\rm dc}/2$.

2) the load power factor is 1, and
3) the peak ac output voltage $V_{\rm o}$ is $V_{\rm dc}$.

Using this assumptions, the theoretical efficiency considers the loss from the active-state MOSFETs only. The theoretical efficiency given by (2) shows that the efficiency of the MCLA with equal capacitor voltages can be improved by increasing the number of H-bridge circuit $k$ only.

The proposed operation controls the MCLA so that the capacitor voltages become unequal to reduce the step voltage. As a result, the theoretical efficiency can be improve without the need to use a large number of H-bridge circuit. The theoretical conversion efficiency of the MCLA with unequal capacitor voltages can be calculated using a similar equation as in (2),

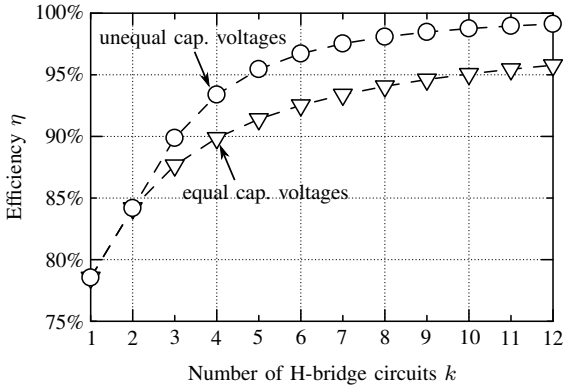


Fig. 7. Theoretical conversion efficiency of MCLA with equal and unequal capacitor voltages.

which is

$$\eta' = \frac{\pi h^2}{2\sum_{j=1}^{l}\sqrt{8hj-4j^2}}, \tag{3}$$

where $h$ is the comparable number of the H-bridge circuit relative to $k$ of the MCLA with equal capacitor voltages for achieving the same theoretical efficiency. $h$ does not represent the actual number of H-bridge circuits. The value of $h$ is given by

$$h = \begin{cases} k, & (1 \le k \le 2) \\ \left(\sum_{j=1}^{k-1} j\right) + 1, & (k > 2). \end{cases} \tag{4}$$

Fig.7 show the plot of the theoretical conversion efficiencies of MCLA with equal and unequal capacitor votlages, and Table V compares the circuit configurations of the MCLA with equal and unequal capacitor voltages at various theoretical efficiencies. The MCLA with equal capacitor voltages reaches the theoretical efficiency of 95.5% using 11 H-bridge circuits, and it requires 56 H-bridge circuits, or 224 MOSFETs, to achieve the efficiency of 99%. This huge number of H-bridge circuits makes the realization of a high conversion efficiency linear power amplifier become impractical. On the other hand, the proposed MCLA with unequal capacitor voltages reaches the theoretical efficiency of 99% by using only 11 H-bridge circuits. Therefore, it may be possible to realize the MCLA with a conversion efficiency close to the theoretical efficiency of 99% by operating the amplifier with unequal capacitor voltages.

## 5. Simulation Results

A simulation was performed to verify the voltage balancing of the MCLA with equal and unequal capacitor voltages and their theoretical conversion efficiencies. The MCLA is constructed using three H-bridge circuits without any filter inductor as shown Fig. 4. Table VI shows the parameters of the MCLA used in the simulation. The on resistance of the MOSFET and forward voltage drop of the body diode are assumed to be zero; thus, the loss is mainly produced by the MOSFETs in the active states.

TABLE V
COMPARISON OF MCLA CONSTRUCTIONS WITH EQUAL AND UNEQUAL CAPACITOR VOLTAGES AT VARIOUS THEORETICAL EFFICIENCIES

| Efficiency | | $\eta$ | 78.5% | 89.9% | 95.5% | 98.1% | 99.0% |
|---|---|---|---|---|---|---|---|
| Equal cell voltages | H-bridge number | $k$ | 1 | 4 | 11 | 29 | 56 |
| | MOSFETs | $4k$ | 4 | 16 | 44 | 116 | 224 |
| | on-state MOSFETs | $2k$ | 2 | 8 | 22 | 56 | 112 |
| Unequal cell voltages | H-bridge number | $k$ | 1 | 3 | 5 | 8 | 11 |
| | MOSFETs | $4k$ | 4 | 12 | 20 | 32 | 44 |
| | on-state MOSFETs | $2k$ | 2 | 6 | 10 | 16 | 22 |

TABLE VI
PARAMETERS OF MCLA FOR SIMULATION

| | | |
|---|---|---|
| Number of H-bridge | $k$ | 3 |
| Capacitors | $C_1$ and $C_2$ | 1800 $\mu$F |
| Load resistor | $R$ | 47 $\Omega$ |
| Capacitor voltage ripple | $V_{\rm r}$ | 1 V |
| Input dc voltage | $V_{\rm dc}$ | 141.4 V |
| Output ac voltage | $v_{\rm o}$ | 100 $V_{\rm rms}$ |

Fig. 8 shows the simulation results of the MCLA. Only the MOSFETs in the main H-bridge circuit are operated in the active state so that the active-state voltages can be compared clearly. $v_{\rm b1}$ and $v_{\rm b2}$ show the MCLA with unequal capacitor voltages reduces the applied voltage across the active-state MOSFETs. The voltage fluctuations of $v_{\rm b2}$, $v_{\rm d2}$, $v_{\rm b3}$, and $v_{\rm d3}$ indicate the transition between switching modes to achieve capacitor voltage balancing. $v_{\rm C1}$ and $v_{\rm C2}$ show that both capacitors achieve voltage balancing since they have constant dc voltages. $\tilde{v}_{\rm C1}$ and $\tilde{v}_{\rm C2}$ are the voltage ripples of $C_1$ and $C_2$. $\tilde{v}_{\rm C1}$ of the MCLA with equal and unequal capacitor voltages are equal to $v_{\rm C1} - V_{\rm dc}/3$ and $v_{\rm C1} - V_{\rm dc}/4$, and $\tilde{v}_{\rm C2}$ of the MCLA with equal and unequal capacitor voltages are equal to $v_{\rm C2} - V_{\rm dc}/3$ and $v_{\rm C2} - V_{\rm dc}/2$. These voltage ripples are well controlled which their amplitudes are equal to $V_{\rm r} = 1$ V. The MCLA with equal and unequal capacitor voltages produce clean sinusoidal waveforms of $v_{\rm o}$ and $i_{\rm o}$. From the simulation, the conversion efficiency of the MCLA with the equal and unequal capacitor voltages are 87.5% and 89.7%, respectively. These efficiencies are nearly identical to the calculated theoretical efficiencies using (2) and (3).

## 6. Conclusion

This paper proposed a new topologies of modular cascade linear amplifier (MCLA) consisting of multiple H-bridge cells and a dc input voltage source. The MCLA is operated as a low noise inductorless inverter. At first, the operation of voltage balancing for the MCLA with equal capacitor voltages was described. Then, the operation of voltage balancing for MCLA with unequal capacitor voltages was proposed. The proposed MCLA with unequal capacitor voltages achieve a higher conversion efficiency than the MCLA with equal capacitor voltages without the need to use a large number of switches. The simulation result verified the voltage balancing of the MCLA with equal and unequal capacitor voltages and their theoretical efficiencies.

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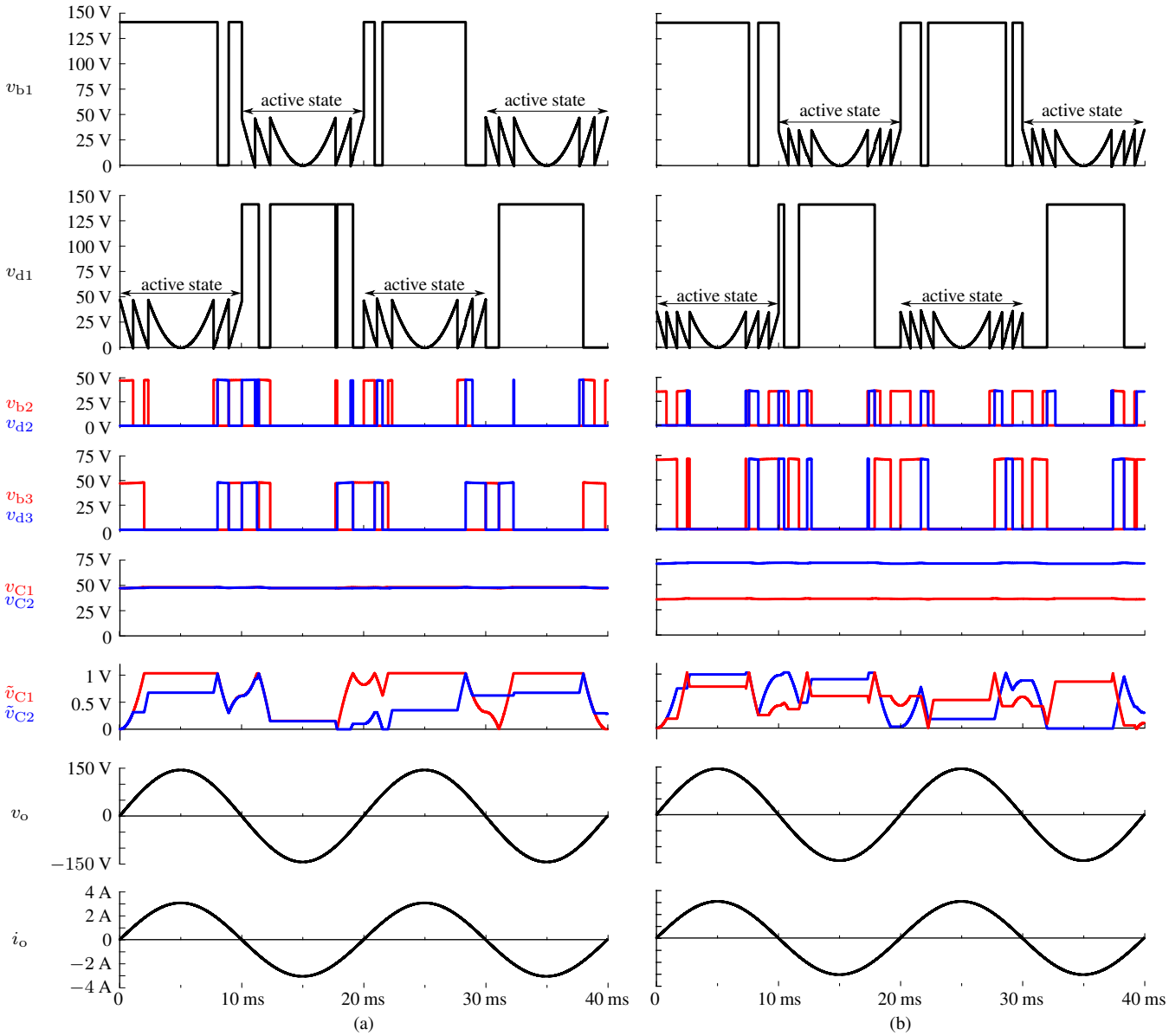


Fig. 8. Simulation waveform of the MCLA consisting of three H-bridge circuits with (a) equal and (b) unequal capacitor voltages.