Implementation of GaN-based HEECS Inverter

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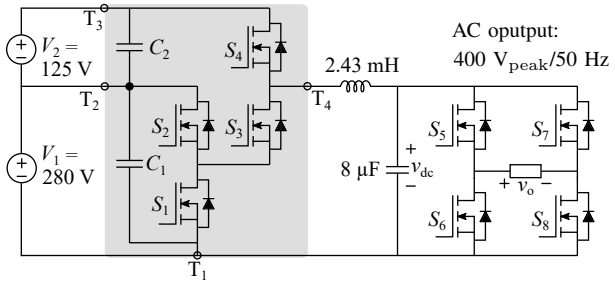


Fig. 1. High efficiency energy conversion system as a power inverter(HEECS)

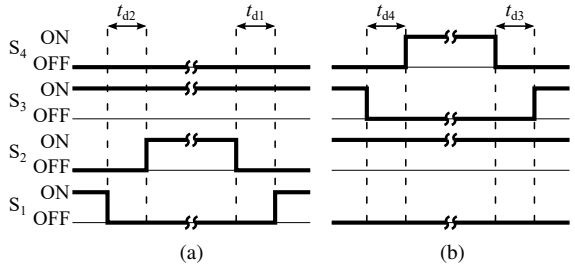


Fig. 2. Gate signals at (a) $0 < v_{\rm dc}^* < V_1$ and (b) $V_1 < v_{\rm dc}^* < V_1 + V_2$

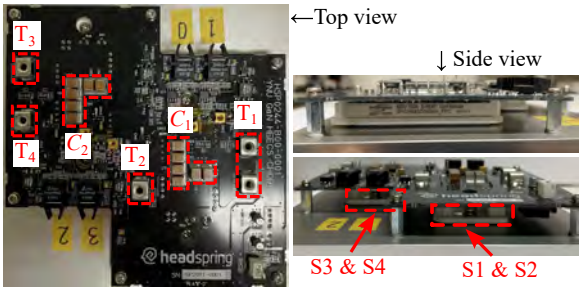
I. High Efficiency Energy Conversion System

This article reports the implementation of a GaN-based high energy conversion system (HEECS) inverter. Fig. 1 shows the circuit configuration of HEECS [1] and the parameters for the experiment. The HEECS comprises a multilevel chopper and an unfolding inverter. The GaN E-HEMTs (GaN Systems:GS-065-150-1-D) are used as the switches S_1 to S_4 of the multilevel chopper. The unfolding inverter comprising S_5 to S_8 was made using low resistance SiC modules (Wolfspeed:CAS325M12HM2) because its switching frequency is 100 Hz.

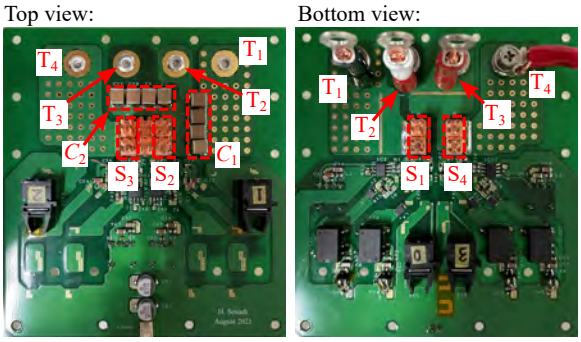
Fig. 2 shows the gate signals to control the output voltage of the multilevel chopper $v_{\rm dc}$. S_1 and S_2 receive PWM signals with a switching frequency of 20 kHz when the chopper output voltage reference $v_{\rm dc}^*$ is less than V_1. At $V_1 < v_{\rm dc}^* < V_1 + V_2$, S_3 and S_4 receive the PWM signals. The deadtimes $t_{\rm d1}$, $t_{\rm d2}$, $t_{\rm d3}$, and $t_{\rm d4}$ are inserted by delaying the ON signals.

II. Construction of Circuit Board

The wide bandgaps semiconductors are known for a fast switching transient resulting in the reduction of the switching loss. To achieve stable operation with a fast switching transient, the inductance of the power loop must be minimized by closely connecting the DC snubber capacitors and the switches operated with complementary



(a)



(b)

Fig. 3. Circuit implementation using (a) half-bridge modules and (b) reflow soldered GaN E-HEMT bare-dies

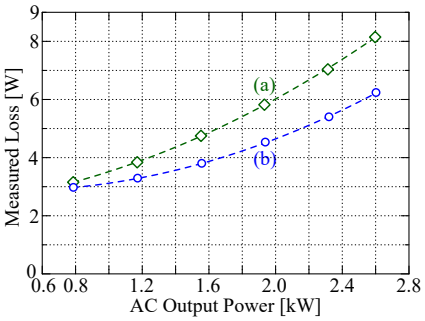
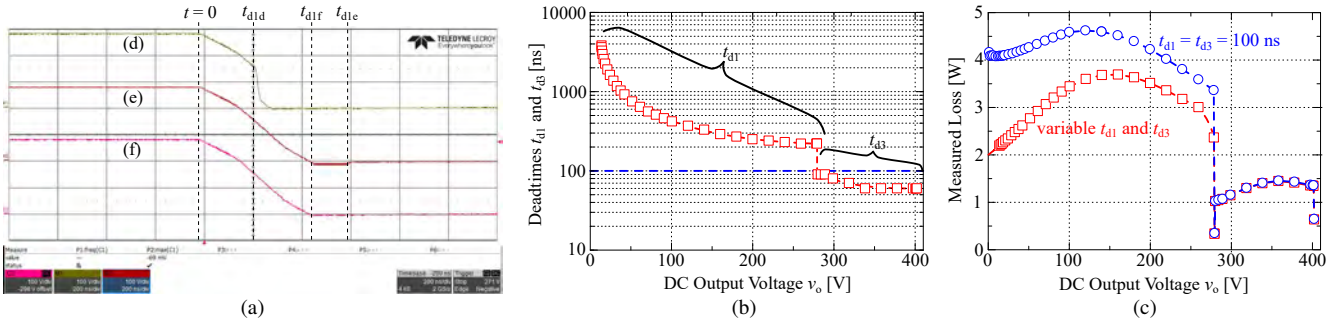


Fig. 4. Measured inverter loss using the circuit comprising (a) half-bridge modules and (b) reflow soldered GaN E-HEMT bare-dies

gate signals. However, many types of multilevel converters built using module packages cannot operate with a fast switching transient because other switches must be connected in the power loop. For example, the primary components for the power loop of the upper half-bridge in Fig. 1 comprises the DC snubber capacitor C_2, and switches S_3 and S_4. However, S_2 must be included in this power loop.

Fig. 3(a) shows the prototype of the multilevel chopper using two half-bridge power modules. Each module comprises two GaN E-HEMTs (GaN Systems:GS-065-150-1-D). C_2 cannot be integrated inside the power module of



(a) (b) (c)

Fig. 5. (a) Drain-to-source voltage of S_1 at $V_o = 100$ V and various deadtimes, (b) selected deadtimes for variable deadtime control, and (c) measured loss at various DC output voltages using load resistor of 100 Ω.

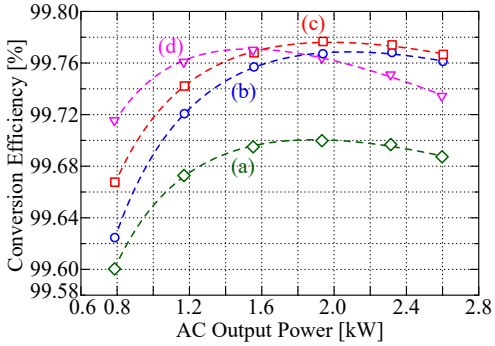


Fig. 6. Measured conversion efficiencies using the circuits comprising (a) half-bridge modules GaN E-HEMT, {(b),(c)} reflow soldered GaN E-HEMT bare-dies, and (d) discrete SiC MOSFETs with {(a),(b)} deadtimes of {(a),(b)} $t_{d2} = t_{d4} = 50$ ns and $t_{d1} = t_{d3} = 100$ ns, (c) $t_{d2} = t_{d4} = 50$ ns and variable t_{d1} and t_{d3}, and (d) $t_{d2} = t_{d4} = t_{d1} = t_{d3} = 200$ ns.

S_3 and S_4, and thus a large inductance of the power loop is inevitable. As a consequence, it is difficult to achieve a stable operation with a fast switching transient. A large ON and OFF gate resistances of 100 Ω and 10 Ω are used to reduce the switching speed.

To create the multilevel chopper with minimum inductance of the power loop, the other prototype was built by reflow soldering the GaN E-HEMT bare-dies (GaN Systems:GS-065-150-1-D) on the PCB. Fig. 3(b) shows the prototype using the reflow soldered GaN E-HEMT bare dies. This prototype uses 5 times smaller gate resistances than the protoype in Fig. 3(a). The used gate drive IC (Skyworks:Si8271AB-IS) limits the minimum usable gate resistances.

The two prototypes were operated to generate 400 V_{peak}/50Hz output. The deadtimes were set at $t_{d2} = t_{d4} = 50$ ns and $t_{d1} = t_{d3} = 100$ ns. Fig. 4 shows the measured losses. The prototype using reflow soldered GaN E-HEMT bare-dies reduces larger power loss at higher output power as the current becomes larger. The power loss reduced by 2 W at 2.6-kW output.

III. Variable Deadtimes Control

The half-bridge chopper can achieve zero voltage switching at the turn-on transition of its lower switch by properly adjusting the delay of the ON signal of the lower switch. Fig. 5(a) shows the drain-to-source voltage of S_1 where the HEECS inverter with a 100-Ω load resistor generated a DC output voltage of 100 V. After S_2 is turned OFF at $t = 0$, the inductor current charges and discharges the output capacitors of S_2 and S_1. The remaining energy stored in the output capacitors is lost if the deadtime is too short t_{d1d}. And S_1 will produce an additional loss owing to a high source-to-drain voltage when the current flows from the source to drain terminal of the GaN E-HEMT if the deadtime is too long t_{d1e}. The proper deadtime is shown by t_{d1f} in Fig. 5(a) where S_1 is turned-ON when its drain-to-source voltage reaches 0 V.

The proper deadtimes for t_{d1} and t_{d3} were measured at various drain currents just before the turn-off transition of S_2 and S_4 and loads. Polynomial interpolations were used to approximate the proper deadtimes, and the polynomial equations were used by the controller to perform variable-deadtimes control. Fig. 5(b) shows the used variable t_{d1} and t_{d3} at various measured DC output votlages. Fig. 5(c) compares the measured losses using $t_{d1} = t_{d3} = 100$ ns and variable deadtimes control. The loss is reduced by half near $v_o = 0$ V as the loss from the output capacitors is reduced by half. The reduction of loss decreases as the current increases.

Fig. 6 compares the measured conversion efficiencies of the two prototypes and the other prototype comprising discrete SiC MOSFETs (ROHM: SCT3017AL). The efficiencies were measured using the direct method [2]. Variable deadtimes control noticeably improves the efficiency at low output power, and the fast switching speed significantly improves the conversion efficiency at high output power. The HEECS inverter comprising reflow soldered GaN E-HEMT bare-dies with variable deadtimes control reached the peak efficiency of 99.78% at 1.94-kW output. This peak efficiency is slightly higher than the peak efficiency of the SiC prototype which is 99.77% at 1.55-kW output.

IV. Conclusion

A GaN-based HEECS inverter has been implemented. The inverter was created by reflow soldering the GaN E-HEMT bare-dies on the PCB to reduce the switching loss. And variable deadtimes control was used to reduce the loss from the output capacitors of the GaN E-HEMTs. The prototype reached the peak conversion efficiency of 99.78% at 1.94-kW output.

References

[1] A. Kawamura, et al, *in Proc. ECCE 2018*, pp. 1308-1313.

[2] A. Kawamura et al, IEEJ JIA, Vol.9, No.6, pp.663-673, 2020 (DOI : 10.1541/ieejjia.20001291).