A Very High Efficiency Circuit Topology for a Few kW Inverter Based on Partial Power Conversion Principle

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***Abstract*—One trend of the fundamental enabling technologies into the direction of the eco-society with more electric power consumption is realization of ultra-high efficiency electric power conversion technologies. In this paper, a very high efficiency circuit topology for a few kW inverter is proposed based on a principle of partial power conversion. The new topology is made of (1) HEECS chopper for full rectified waveform generation and (2) unfolding full bridge inverter for full sinusoidal wave synthesis. The theoretical efficiency is derived, and the preliminary experimental verification confirmed the efficiency expectation. Tentatively, 99.2% efficiency was measured for the DC-to-full-rectified-waveform conversion at 3.6 kW output.**

***Index Terms*—high efficiency inverter, partial power conversion, wide band gap devices**

I. Introduction

One trend of the fundamental enabling technologies into the direction of eco-society with more electric power consumption is realization of ultra-high efficiency electric power conversion technology, which enables the super energy saving and increases the more use of electric energy in the future eco-society [1]–[4]. Using SiC devices and a special circuit topology, a very high efficiency was reported in [8], in which over 99.5% efficiency was experimentally verified with a DC-DC chopper (350 Vdc, 3 kW output power). The basic principle is called a partial voltage boost in this literature. This is only for the DC-DC conversion, thus a very high efficiency DC-AC conversion is also required toward the future.

Many researchers are studying on the high efficiency inverter [5]–[7]. In [5], a flying capacitor transformerless inverter with common ground for a grid connected solar photovoltaic system was proposed. The proposed system has only four power switches and small filter, and achieved 99.2% efficiency at 1 kW. In [6], L. Zhang et al. designed an asymmetrical interleaved full-bridge inverter for google little box challenge. They obtained 99.3% efficiency at 2 kW by using GaN switching devices. T. Miyazaki et al. have proposed a trans-linked interleaved inverter [7]. Two phase are trans-linked each other in order to reduce the smoothing inductance. As a result, the loss could be reduced, and 99.4% efficiency was achieved at 2 kW.

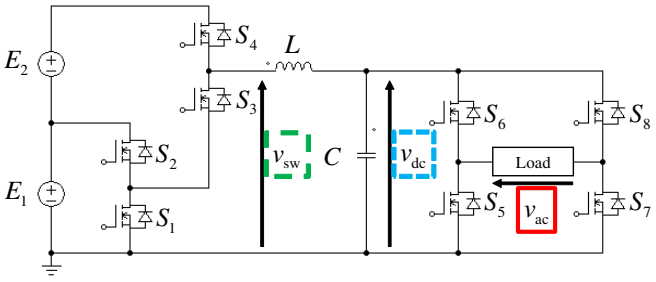

Fig. 1. Proposed 2 battery HEECS inverter.

This paper proposes a very high efficiency circuit topology for a few kW inverter based on the principle of "partial power conversion", which is modified from [8]. To some extent, this topology is similar to a T-type three level converter [9]. Wide band gap (WBG) switching devices such as SiC and GaN are also used in the proposed circuit. Over 99.5% efficiency is challenged in a few kW power range. In Section II, this new topology is proposed, and the possible theoretical highest efficiency is derived for this topology. In Section III, implementation problems of the chopper control is described.. In Section IV, experimental verification is reported. This paper is concluded in Section V.

II. Proposal of a New Ultra-High Efficiency Inverter Topology

This section explains the new ultra-high efficiency inverter topology and the theoretical efficiency calculations.

A. Proposed Topology and Principle of "Partial Power Conversion"

Fig. 1 depicts the proposed topology, which is based on the principle of "Partial Power Conversion", and named as 2 battery HEECS inverter. The first power stage of this converter is similar to the 2 battery HEECS chopper in [8], which has two batteries and each battery has special connection to buck converters. HEECS stands for "High Efficiency Energy Conversion System" [8]. When the output voltage command

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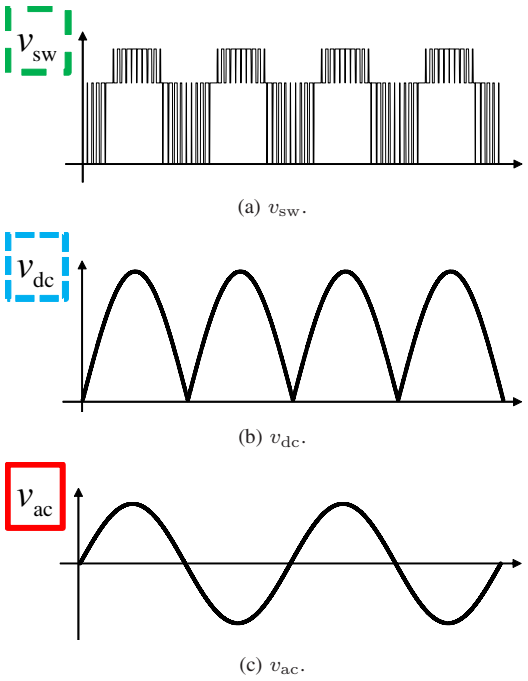
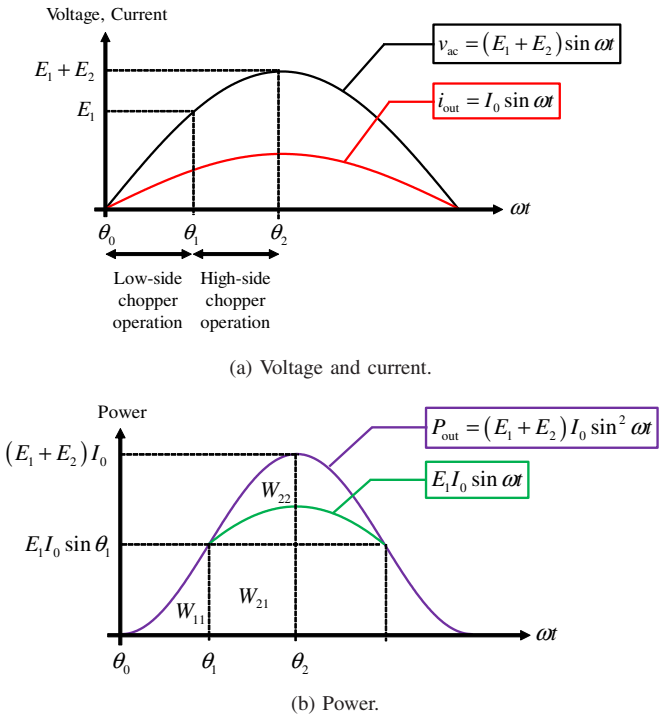


(a) $v_{\rm sw}$.

(b) $v_{\rm dc}$.

(c) $v_{\rm ac}$.

Fig. 2. Voltage waveforms at three different points.



(a) Voltage and current.

(b) Power.

Fig. 3. Waveforms in a half cycle.

is below the battery♯1 voltage E_1, only switches S_1 and S_2 operates and lower buck converter generates PWM output voltage, while the switch S_3 is always in "on state". When the output voltage command is between E_1 and (E_1+E_2), where E_2 is the battery♯2 voltage, then the switch S_2 is always in "on state" and the upper buck converter generates PWM waveform. As a result, a typical waveform of the output voltage $v_{\rm sw}$ in Fig. 1 is illustrated in Fig. 2(a), where the output voltage command is a full rectified waveform.

Through the LC filter shown in Fig. 1, the filtered output voltage $v_{\rm dc}$ is controlled so that a half sinusoidal waveform is synthesized as shown in Fig. 2(b). A special PWM control called deadbeat control is applied for both buck converters and it will be explained in subsection III-A [12].

In the second power stage, a unfolding inverter unfolds the half sinusoidal waveform into the full sinusoidal waveform. The final voltage $v_{\rm ac}$ is illustrated in Fig. 2(c). The unfolding inverter changes the switching mode once in a half cycle.

This topology is derived as a result of pursuing the higher power conversion efficiency. When the 2 battery HEECS chopper, which is the first stage of the 2 battery HEECS inverter, is operating for the constant DC output voltage command below E_1, only lower buck converter operates and the switch S_3 is always in "on state". Under this condition, if the lower buck chopper efficiency is defined as $\eta_{\rm lower}$, and the conduction loss of S_3 is ignored, the HEECS chopper efficiency $\eta_{\rm chop-L}$ becomes

$$\eta_{\rm chop-L}=\eta_{\rm lower}. \tag{1}$$

When the output dc voltage command is between E_1 and (E_1+E_2), the upper buck converter operates keeping the switch S_2 in "on state". Ignoring the conduction loss of switch S_2, and defining the output power of battery♯1 and battery♯2 and the efficiency of the upper buck converter as P_1, P_2, and $\eta_{\rm upper}$, respectively, the HEECS chopper efficiency $\eta_{\rm chop-H}$ can be approximately expressed as follows:

$$\eta_{\rm chop-H}=\frac{P_1+\eta_{\rm upper}P_2}{P_1+P_2}. \tag{2}$$

(2) implies that if the power P_2 becomes smaller, then the efficiency $\eta_{\rm chop-H}$ becomes higher than $\eta_{\rm upper}$ and it approaches to 1.0, because P_2, which is the power corresponding to the output voltage above E_1, is converted at the upper buck converter and the switch S_2 of the lower buck converter is always "on state". This is the basic idea of the principle of "Partial Power Conversion" [8]. The HEECS topology is based on this principle, which has potential for very high efficiency.

Also, as for the unfolding inverter, if the conduction loss is very small, the total power conversion loss should be very small, because the switching loss is negligible due to one switching in a half cycle.

In the next subsection, efficiency optimization of two power stages is discussed when the output voltage command is sinusoidal.

B. Theoretical Highest Efficiency for AC Operation

When the output voltage command is sinusoidal, we have several kinds of freedom for aiming at higher efficiency.

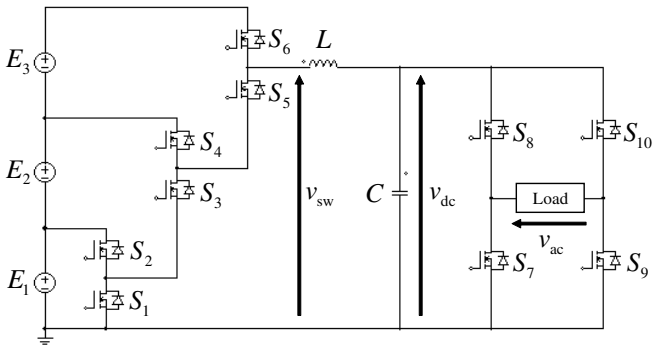


Fig. 4. 3 battery HEECS inverter.

1) Optimization of Battery Voltage E_1 and E_2: When the output voltage command of the first stage HEECS chopper is ac sinusoidal, the average efficiency can be theoretically calculated by integrating the efficiency of (1) and (2) through one cycle and averaging it. Fig. 3(a) is a waveform of a half cycle HEECS chopper output voltage and current under an assumption of a pure resistive load. The horizontal axis is the electrical angle. θ_0 is the beginning angle of this cycle and is set to 0 degree. θ_1 is the angle when the upper chopper starts the PWM operation and the lower chopper switch S_2 is always "on state". θ_2 is 90 degrees. Energy [J] transmitted from the battery to the load is defined in Fig. 3(b). The total energy [J] from battery♯1 during [θ_0, θ_1] is defined as W_{11} The total energy from battery♯1 and battery♯2 during [θ_1, θ_2] are defined as W_{21} and W_{22} respectively. Based on these definitions, if the other losses such as conduction loss are ignored, the quarter cycle average efficiency of HEECS chopper is given as

$$\eta_{\text{chop}} = \frac{W_{11} \times \eta_{\text{lower}} + W_{21} + W_{22} \times \eta_{\text{upper}}}{W_{11} + W_{21} + W_{22}}. \quad (3)$$

For the further optimization analysis, it is assumed that the efficiency of two chopper is identical, then (3) becomes

$$\eta_{\text{chop}} = \frac{(W_{11} + W_{22}) \times \eta_{\text{upper}} + W_{21}}{W_{11} + W_{21} + W_{22}}. \quad (4)$$

Looking at (4), if the chopper efficiency η_{upper} is given, the highest efficiency η_{chop} can be obtained when W_{21} in (4) is maximized. Using the relation of $(E_1 + E_2)\sin\theta_1 = E_1$, W_{21} is calculated as

$$W_{21} = \int_{\theta_1}^{90} (E_1 + E_2)\sin\theta_1 I_0 \sin\theta d\theta \quad (5)$$

After a simple manipulation, (5) becomes

$$W_{21} = (E_1 + E_2)\, I_0 \sin\theta_1 \cos\theta_1. \quad (6)$$

Thus, when θ_1 is 45 degrees, W_{21} is maximized. The ratio of the voltage E_1 and E_2 becomes $E_1 \simeq 2.41E_2$.

Based on the above idea, multiple battery HEECS inverter can be possible. For example, three battery HEECS inverter topology is illustrated in Fig. 4. The maximized efficiency is obtained when the three batteries are switched at 12.6 degrees and 58.3 degrees after a short calculation.

TABLE I
RATING OF THE TARGET INVERTER AND PARAMETERS USED IN THIS PAPER FOR HEECS CHOPPER.

Output voltage (rated)	400 V_{peak}
Output current (rated)	25 A_{peak}
Load resistance (rated 5 kW)	16.6 Ω
Filter inductance	585 μH
Filter capacitance	80 μF
Frequency of sinusoidal output	50 Hz
Power device (chopper)	SCT3017AL (Rohm)

2) Selection Criteria of Switching Devices at Chopper and Unfolding Full Bridge Inverter: The efficiency of the first stage of the HEECS inverter can be maximized by selecting proper WBG devices with less switching loss. Additionally, the efficiency of the unfolding inverter can be also optimized by selecting a proper switching device with low conduction loss. The proper parameters selection is under investigation, however, Table I shows the parameters of the targeted inverter power rating and the tentative components.

III. Implementation Problems – Control of Chopper

This section describes the implementation problems for the chopper control.

A. Deadbeat Control of Output Voltage

To achieve a very accurate output voltage synthesis, a deadbeat control is applied [10]–[12]. The deadbeat control is one of digital control methods. The output voltage should be controlled as a half sinusoidal waveform shown in Fig. 2(b). The deadbeat control is effective, because the output voltage can be quickly controlled. The detailed derivation for the control law and the practical problems and the solutions can be found in [12].

The control law is derived from the discrete state equation of a DC-DC buck converter, which is expressed as

$$\dot{\boldsymbol{x}}\,[k+1] = \boldsymbol{F}\boldsymbol{x}\,[k] + \boldsymbol{G}\Delta T\,[k] \quad (7)$$

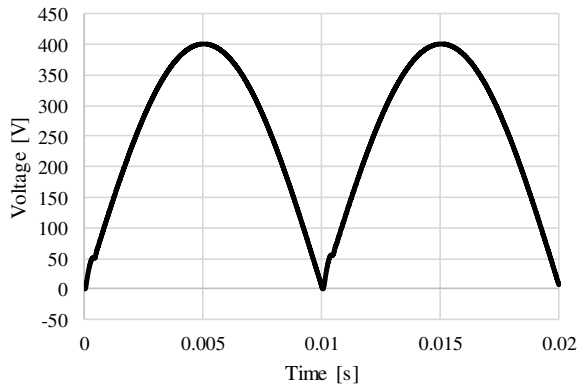
where

$$\boldsymbol{x}\,[k] = \begin{bmatrix} v_{\text{dc}}[k] \\ i_{\text{L}}[k] \end{bmatrix},$$

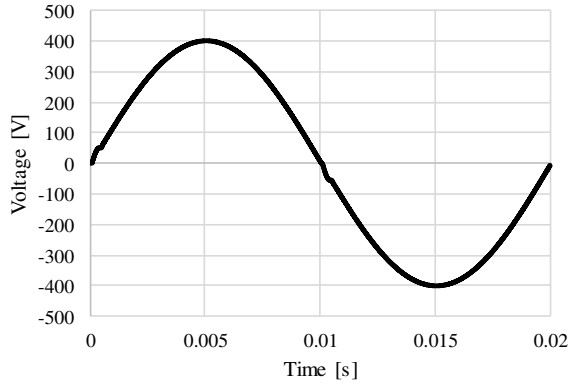
$$\boldsymbol{F} = e^{\boldsymbol{A}T} = \begin{bmatrix} F_{11} & F_{12} \\ F_{21} & F_{22} \end{bmatrix}, \boldsymbol{G} = e^{\boldsymbol{A}T}\boldsymbol{B}E = \begin{bmatrix} g_1 \\ g_2 \end{bmatrix}. \quad (8)$$

$\Delta T[k]$ is the time when the switch is on in one switching period. The state variable $\boldsymbol{x}[k]$ consists of the capacitor voltage v_{dc} and inductor current i_{L}. E is the input dc voltage of the DC-DC buck converter. $\boldsymbol{A}$ and $\boldsymbol{B}$ denote the state matrix and input matrix of the continuous state equation, respectively. Assuming that the load is a resistor R, $\boldsymbol{A}$ and $\boldsymbol{B}$ are derived as

$$\boldsymbol{A} = \begin{bmatrix} -1/CR & 1/C \\ -1/L & 0 \end{bmatrix}, \boldsymbol{B} = \begin{bmatrix} 0 \\ 1/L \end{bmatrix}. \quad (9)$$



(a) Full rectified waveform.



(b) Unfolded sinusoidal output voltage.

Fig. 5. Simulated waveforms of 2 battery HEECS inverter. (E_1 = 280 V, E_2 = 140 V)

In the first row of (7), by replacing $v_{\rm dc}[k+1]$ with the reference voltage $v_{\rm ref}$ and solving for $\Delta T[k]$, the deadbeat control law can be derived as

$$\Delta T[k] = \frac{1}{g_1}\left(v_{\rm ref} - F_{11}v_{\rm dc}[k] - F_{12}i_{\rm L}[k]\right). \qquad (10)$$

B. Simulations

This subsection describes the simulation results of the output sinusoidal wave generation. The simulations were conducted by using PSIM produced by Powersim Inc. The simulation results are shown in Fig. 5, which are (a) a full rectified waveform and (b) the unfolded sinusoidal output voltage. The simulation parameters are the same as Table I. From the simulation results, it was confirmed that the deadbeat control can generate the full rectified waveform. Additionally, the unfolding inverter successfully generated the sinusoidal output voltage.

IV. Verification Experiments and Discussions

A. Efficiency of 2 Battery HEECS Chopper

The 2 battery HEECS inverter was constructed using the circuit parameters shown in Table I. The deadbeat controller

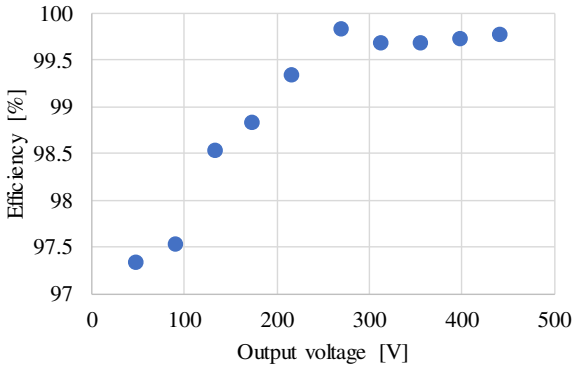


Fig. 6. Measured efficiency of 2 battery HEECS chopper. (E_1 = 270 V, E_2 = 180 V, 66.6 Ω load)

was implemented into this circuit. Then several characteristics were measured. The efficiency was measured using a power analyzer "PW6001" produced by Hioki E. E. Corporation.

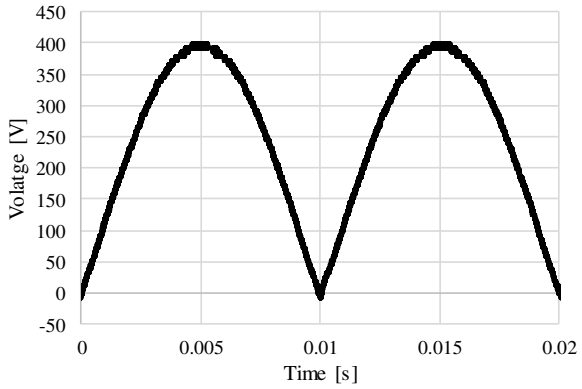
First the efficiency of the DC-DC conversion part of the 2 battery HEECS inverter was measured, when the output voltage is a constant dc voltage. Fig. 6 is the measured efficiency of 2 batery HEECS chopper on a case that E_1 and E_2 are 270 V and 180 V. The horizontal axis is the output dc voltage and the vertical axis is the measured efficiency. A high efficiency was measured as we analyzed in Section II.

Second, the output voltage command was changed to a full rectified waveform under deadbeat control, and the efficiency was measured. The output voltage waveforms are shown in Fig. 7, which are (a) a full rectified sinusoidal waveform and (b) the unfolded sinusoidal output voltage. The measured efficiency at a full rectified waveform was shown in Fig. 8. The highest power conversion efficiency is 99.2% at the 3.6 kW output. The ac output voltage was confirmed in Fig. 7(b) after the unfolding full bridge inverter.

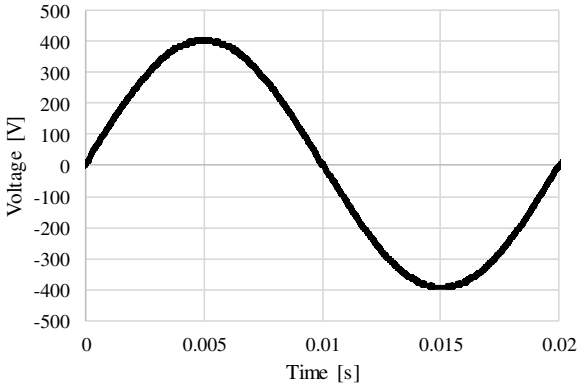
B. Discussions

The loss in Fig. 8 may be categorized to: (1) power device switching loss, (2) power device conduction loss, (3) inductance loss (conduction loss + iron loss), (4) capacitance loss, (5) others [7]. Also the unfolding inverter loss is added if the loss is measure at the ac load side. The switching loss should be minimized based on the proposed HEECS inverter topology. However, due to the controllability of the deadbeat control law, E_1 and E_2 in the experiment is not equal to the ideal E_1 to E_2 voltage ratio mentioned in subsection II-B.

In general, the following may be a remedy for the higher efficiency for HEECS inverter; smaller filter C, reduction of the ripple current in inductor, and the best combination of the switching loss and the conduction loss. The inductor current waveform is shown in Fig. 9(a), in which relatively large current ripples are observed. This can be reduced by the proper selection of the LC filters and tuning of the deadbeat control law. Fig. 9(b) shows the HEECS chopper dc output waveform before the LC filter $v_{\rm sw}$ in Fig. 2(a). It is controlled based on the deadbeat control law. It was confirmed that the HEECS



(a) Full rectified waveform.



(b) Unfolded sinusoidal output voltage.

Fig. 7. Experimental waveforms of 2 battery HEECS inverter. (E_1 = 280 V, E_2 = 140 V, 2.5 kW output)

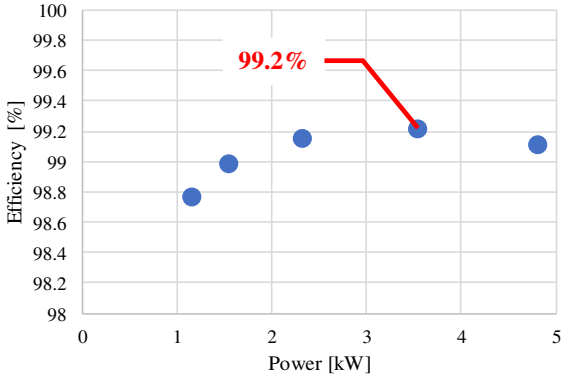
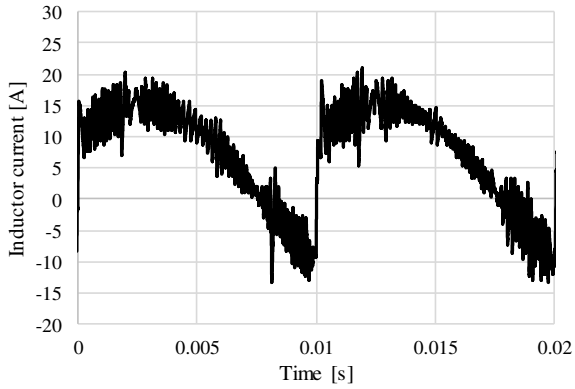
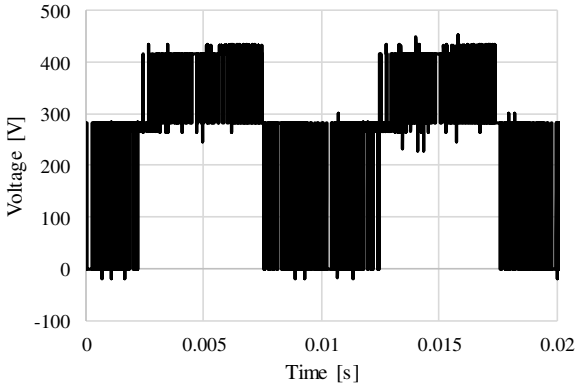


Fig. 8. Measured efficiency of 2 battery HEECS chopper with half sinusoidal waveform output. (E_1 = 280 V, E_2 = 140 V, 400 Vpeak output voltage)

chopper dc output waveform before the LC filter was similar to Fig. 2(a).



(a) Inductor current i_{L}.



(b) HEECS chopper dc output waveform before the LC filter v_{sw} in Fig. 2(a).

Fig. 9. Experimental waveforms of inductor current and HEECS chopper dc output. (E_1 = 280 V, E_2 = 140 V, 2.5 kW output)

V. Conclusions

Based on a new principle - "partial power conversion", a new topology for high efficiency inverter is proposed using WBG devices. From the theoretical efficiency calculation, a very higher efficiency is expected in a few kW power range. The theoretically highest efficiency is derived for this circuit topology. Simulations and experiments were done for verifications. Tentatively, 99.2% efficiency was measured for the DC-to-full-rectified-waveform conversion at 3.6 kW output. Several improvements are expected for higher efficiency by redesign of the LC filter, implementation of the deadbeat control, and selection of the battery voltage ratio E_1/E_2.

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