Discussion on Loss Breakdown of 99.6% Efficiency Two Battery HEECS Inverter

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Keywords

≪Voltage Source Inverter (VSI)≫, ≪Efficiency≫, ≪Measurement≫, ≪Multilevel Converters≫

Abstract

A very high efficiency HEECS topology inverter was proposed at ECCE2018, and after several modifications a very high efficiency 99.6% is observed at approximately 2.3 kW output. In this paper, the loss breakdown is summarized and the possibility for the higher efficiency is discussed based on the loss analysis.

1 Introduction

By development of wide-band-gap power devices such as SiC and GaN, the power conversion efficiency is improved and the heat dissipation is reduced. As a result, several papers have been published on the higher power density from google little box challenge [1][2]. On the other hand, the pursue of the highest efficiency close to 100% is also interesting target from the view point of science. In [3], 99.4% efficiency was reported at 2 kW output. A question: on what reason or on what cause the power conversion efficiency cannot reach 100%, this is important when the higher power density is pursued. Authors have proposed a new topology for a few kW HEECS inverter suitable for the SiC and the tentative high efficiency was reported in [4]. After several improvements, 99.6% power conversion efficiency was measured at 400 Vpeak, 2.2 kW output power. A loss analysis is described in this paper and the accuracy of the measurement is clarified.

In the section 2, a brief summary of the two battery HEECS inverter is explained, and the measured high efficiency is illustrated in the sections 3. The section 4 is discussion of the loss breakdown, in which first the loss of DC output operation is discussed based on the measured data, and second the AC operation is discussed and AC losses in the passive components will be investigated. Third, accuracy of the proposed measurement approach is discussed, and the reasonable value is proposed. The section 5 concludes this paper.

2 Two battery HEECS Inverter

Fig. 1 depicts the proposed topology, which is based on the principle of “Partial Power Conversion”, and named as two battery HEECS inverter[4]. The first power stage of this converter is similar to the two battery HEECS chopper in [5], which has two batteries and each battery has special connection to buck converters. HEECS stands for “High Efficiency Energy Conversion System” [5]. When the output

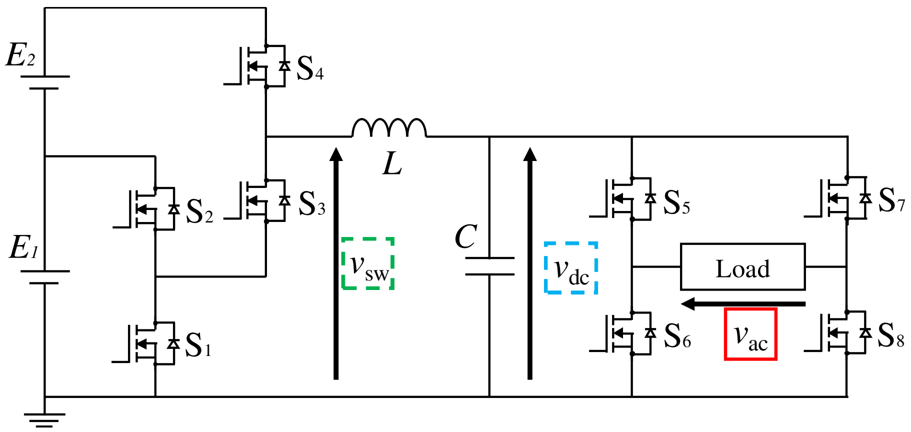
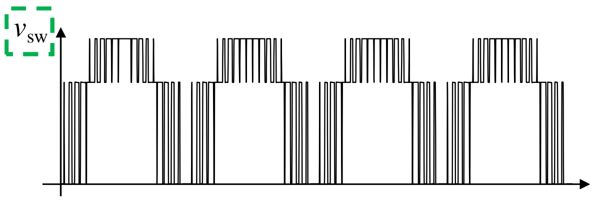


Fig. 1: Circuit of two battery HEECS inverter.

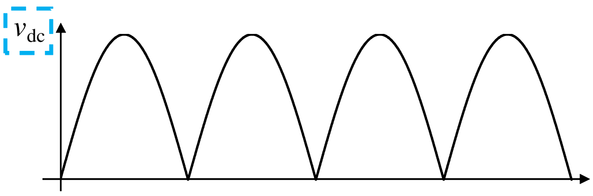
voltage command is lower than the battery ♯ 1 voltage E_1, only switches S_1 and S_2 operates and lower buck converter generates PWM output voltage, while the switch S_3 is always in “on state”. When the output voltage command is between E_1 and (E_1+E_2), where E_2 is the battery ♯ 2 voltage, then the switch S_2 is always in “on state” and the upper buck converter generates PWM waveform. As a result, a typical waveform of the output voltage v_{sw} in Fig. 1 is illustrated in Fig. 2(a), where the output voltage command is a full rectified waveform.

Through the LC filter shown in Fig. 1, the filtered output voltage v_{dc} is controlled so that a full rectified waveform is synthesized as shown in Fig. 2(b).

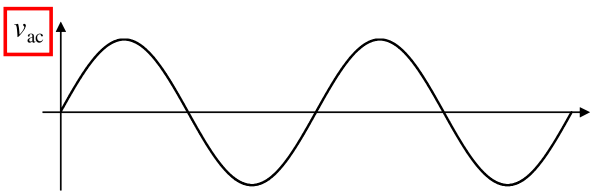
In the second power stage, an unfolding inverter unfolds the full rectified waveform into the complete sinusoidal waveform. The final voltage v_{ac} is illustrated in Fig. 2(c). The unfolding inverter changes the switching mode once in a half cycle, thus the switching loss is negligible. The total efficiency can be optimized by the proper selection of E_1 and E_2[4].



(a) v_{sw}.



(b) v_{dc}.



(c) v_{ac}.

Fig. 2: Waveforms of two battery HEECS inverter.

ISBN: 978-9-0758-1530-6 - IEEE catalog number: CFP19850-USB

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Table I: Specifications and circuit parameters of HEECS inverter.

Output voltage (rated)	400 V_{peak}
Output cuurent (rated)	25 A_{peak}
Load resistance (rated 5 kW)	16.6 Ω
Lower voltage source	280 V
Upper voltage source	125 V
Filter inductor (amorphous)	2.43 mH
Conduction resistance of inductor	6.24 mΩ
Filter capacitor	8 μF
ESR of capacitor	3.5 mΩ
Frequency of sinusoidal output	50 Hz
Frequency of Switching	20 kHz
Deadtime	200 ns
Power device (chopper)	SCT3107AL (Rohm)
Conduction resistance of device (chopper)	17 mΩ (typ.)
Power device (inverter)	BSM180D12P2C (Rohm)
Conduction resistance of device (inverter)	12 mΩ (typ.)

Table II: List of measurement instruments.

Power analyzer	PW6001 (HIOKI)
Voltage range	6 V ~ 1500 V
Current range	400 mA ~ 20 A
Voltage accuracy	±0.02 % rdg. ±0.02 % f.s.
Current accuracy	±0.02 % rdg. ±0.02 % f.s. +probe error
Power accuracy	±0.02 % rdg. ±0.03 % f.s. +probe error
Current probe	CT6841-05 (HIOKI)
Rated current	AC/DC 20 A
Characteristic for freq.	Amplitude: DC ~ 1 MHz Phase: DC ~ 300 kHz
Current accuracy (DC)	±0.02 % rdg. ±0.05 % f.s.
Current accuracy (~ 100 Hz)	±0.3 % rdg. ±0.01 % f.s., ±0.1°
Oscilloscope	Wavesurfer 3024 (TELEDYNE LECROY)
Voltage probe	HVD3206
Current probe	CP030

3 Measurement

3.1 Specifications of 5 kW two battery HEECS Inverter

The specifications of the prototype of 5 kW HEECS inverter is summarized in Table I, where the highest possible efficiency is the target of this research, thus the power density is not considered this time. The target output rating is selected to be single phase 400 Vpeak, 25 Apeak and 5 kW at the 20 kHz switching frequency. The output is supposed to be connected to the utility grid, and a pure AC output voltage is assumed.

3.2 Measurement Instruments

The measurement methodology may be called direct loss subtraction calculation, in which the total input power and the total output power are measured and the subtraction is assumed to be a loss. This method may cause a large error if the accuracy of the all measurement are not guaranteed to be high. The accuracy will be discussed in section 4. All instruments used for this measurement are summarized in Table II.

3.3 Efficiency measurement

Fig. 3(a) is the measured efficiency of the HEECS inverter, in which the horizontal axis is the output power and the vertical axis is efficiency. It is observed that the efficiency reaches 99.6% at around 2.3 kW output power. The input power was measured by the sum of two DC voltage source power, and the output power at the load resistance was measured at 400 Vpeak. The loss was estimated by the subtraction of two measured data, and the Fig. 3(b) shows the absolute value of the loss in [W].

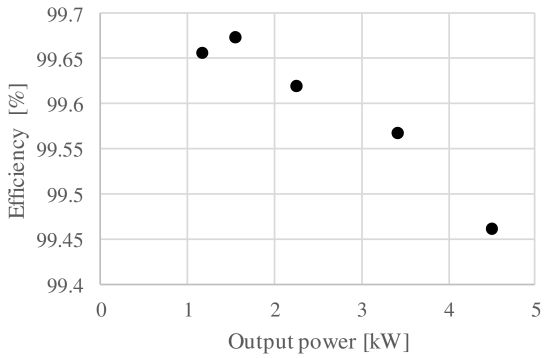
In general, the HEECS inverter in Fig. 1 has the following kinds of losses.

(1) losses in the HEECS chopper

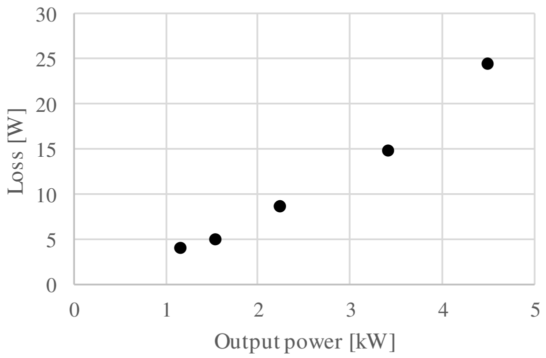
- 1-1 turn-on switching loss
- 1-2 turn-off switching loss
- 1-3 conduction loss of the power devices
- 1-4 resistance loss in printed copper patterns at PCB

(2) passive components losses

- 2-1 inductor loss (copper loss, fundamental frequency (50 Hz) iron loss, harmonic iron loss)

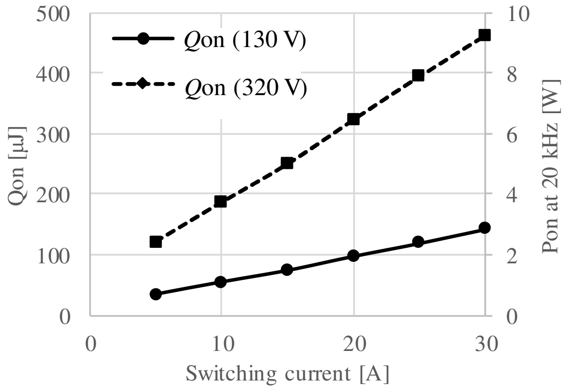


(a) AC output measured efficiency of HEECS inverter.

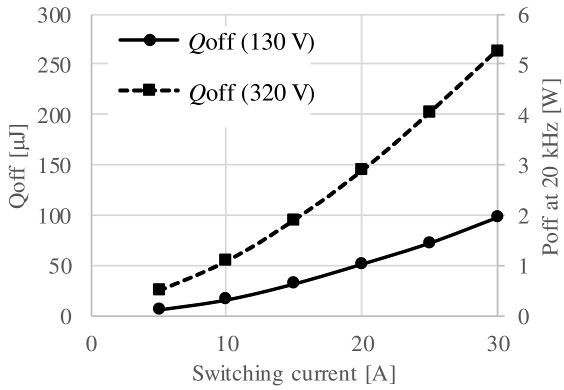


(b) Loss measurement of AC output HEECS inverter.

Fig. 3: Measured result of 2 HEECS inverter. ($E_1 =$ 280 V, $E_2 = 125$ V, 400 Vpeak AC output voltage)



(a) Turn-on loss of power device SCT3017AL.



(b) Turn-off loss of power device SCT3017AL.

Fig. 4: Measured loss by two-pulse-testing.

  2-2 capacitor loss (ESR loss)

(3) unfolding inverter losses

  3-1 conduction loss

  3-2 switching loss

  3-3 resistance loss in connection line

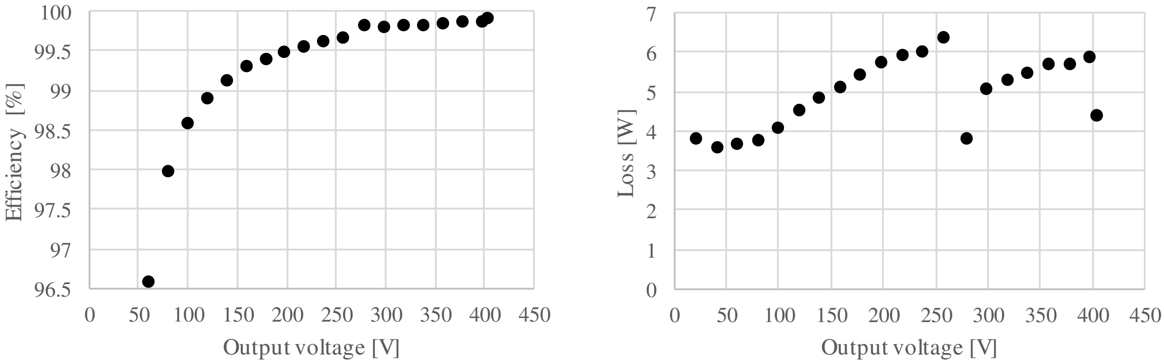
(4) stray losses

The inverter changes its output operating point in sinusoidal manner, thus it is difficult to identify the theoretical loss breakdown. In the following section, these kinds of losses are estimated in three operation modes, which are (a) no switching DC operation, (b) DC -DC operation, and (c) DC-AC operation.

4 Discussions

4.1 Two-pulse switching loss measurement

The switching loss of power device can be measured by “two-pulse-testing” method [6][7]. The voltage and the current are selected to be in the similar range of the operation in 5 kW. The measured data are shown in Fig. 4(a) and Fig. 4(b), in which the turning-on loss is shown in Fig. 4(a) and Fig. 4(b) is on the turning-off loss. These values are a little larger than those in the data sheet provided by the device maker. The transient characteristics of the power devices depend on the hardware design of the gate circuit and also hardware design of the power circuit, thus the obtained data may be reasonable.



(a) DC output measured efficiency of HEECS chopper.

(b) Loss measurement of DC output HEECS chopper.

Fig. 5: Measured result of 2 HEECS inverter. (($E_1 = 279.6$ V, $E_2 = 124.4$ V, $R = 33.3\ \Omega$), DC output voltage)

4.2 DC output operation and loss measurement

First, the loss is measured under the different DC output voltage, when the output DC voltage is changed under DC-DC operation. Fig. 5(a) is the efficiency and Fig. 5(b) is the absolute value at the loss.

From these figures, the interesting fact can be confirmed, which is the loss at output voltage $v_{ac} = E_1 + E_2$, and also at output voltage $v_{ac} = E_1$. Due to the basic principle of the HEECS chopper, on the above two operation modes, no switching occurs. For example, when the output voltage is equal to $E_1 + E_2$, both the lower chopper switches S_1 and S_2 are off and only high side switch of the chopper S_4 is continuously on. Thus, under this mode, the loss is only the conduction loss of the switching device and inductor.

The measured loss (or efficiency) can be compared with the theoretically calculated loss (or efficiency) in Table III. The upper table depicts the measured loss by the direct method. The loss is calculated by the subtraction of output power from the input power. The lower table depicts the theoretically calculated loss based mainly on the measured data, which are switching loss, device conduction loss, PCB conduction loss, inductor fundamental frequency iron loss, inductor ripple frequency iron loss, and inductor conduction loss. No switching occurred in this table, thus the switching loss, fundamental frequency iron loss and ripple frequency iron loss are set to be zero. The PCB conduction resistance and effective conduction loss of four SiC switches depend on the switching pattern, thus the PCB equivalent line resistance is calculated depending on the duty ratio. The PCB line resistance is obtained by the network analyzer and confirmed by the circuit simulator calculation. These parameters are listed in Table IV.

Table III: Loss breakdown at DC operation without switching. ($E_1 = 279.6$ V, $E_2 = 124.4$ V, $R = 33.3\ \Omega$)

Measured loss								
Duty	E_1 [V]	E_2 [V]	V_{out} [V]	I_{dc} [A]	Output power [W]	Total loss [W]	Efficiency [%]	Effective duty
$d_{up} = 1.0$	279.6	124.4	403.3	11.49	4637	4.4	99.91	0.9983
$d_{low} = 1.0$	279.7	124.8	279.1	7.97	2224	3.8	99.83	0.9979

Calculated loss											Error rate meas. vs calc.
Power device			Inductor			Line resistance			Estimated total loss	Efficiency	
$P_{SW\text{-}on}$ [W]	$P_{SW\text{-}off}$ [W]	$r_{on}I_{dc}^2$ [W]	$r_L I_{dc}^2$ [W]	Iron loss of 50 Hz [W]	Iron loss of [W]	Upper [mΩ]	Middle [mΩ]	Loss [W]	[W]	[%]	[%]
0	0	2.38	0.82	0	0	6.4	0	0.84	4.05	99.91	-8.07
0	0	2.29	0.4	0	0	0	8.8	0.56	3.24	99.85	-14.9

Table IV: Parameters in Table.III.

Device on resistance	r_{on} [mΩ]	18
Inductor resistance	r_L [mΩ]	6.24
Line resistance (upper: S_4 is on.)	r_{lup} [mΩ]	6.4
Line resistance (middle: S_2 and S_3 are on.)	r_{lmd} [mΩ]	8.8
Line resistance (lower: S_1 and S_3 are on.)	r_{ldwn} [mΩ]	8.8

Table V: Loss breakdown at DC operation with switching. ($E_1 = 279.6$ V, $E_2 = 124.4$ V, $R = 33.3$ Ω)

Measured loss								
Duty	E_1 [V]	E_2 [V]	V_{out} [V]	I_{dc} [A]	Output power [W]	Total loss [W]	Efficiency [%]	Effective duty
$d_{up} = 0.95$	279.6	124.5	397.6	11.32	4502	5.9	99.87	0.9478
$d_{up} = 0.79$	279.7	124.5	377.9	10.77	4070	5.7	99.86	0.7888
$d_{up} = 0.47$	279.7	124.5	338.4	9.661	3270	5.5	99.83	0.4715
$d_{low} = 0.70$	279.7	124.5	198.2	5.69	1127	5.8	99.49	0.7086
$d_{low} = 0.49$	279.7	124.5	139.0	3.99	555.6	4.8	99.13	0.497

Calculated loss													Error rate meas. vs calc. [%]
Power device				Inductor			Line resistance			Estimated total loss	Efficiency		
$P_{SW\text{-}on}$ [μJ]	$P_{SW\text{-}off}$ [μJ]	P_{on+off} [W]	$r_{on}I_{dc}^2$ [W]	$r_L I_{dc}^2$ [W]	Fund-comp iron loss [W]	Ripple-comp iron loss [W]	Upper [mΩ]	Middle [mΩ]	Loss [W]	[W]	[%]		
65	20	1.7	2.43	0.8	0	0.2	6.53	0	0.84	5.96	99.87		1.064
60	17	1.54	2.53	0.72	0	0.6	6.9	0	0.8	6.19	99.85		8.665
55	15	1.4	2.57	0.58	0	0.6	7.67	0	0.72	5.87	99.82		6.656
120	25	2.9	1.16	0.2	0	1.8	0	8.8	0.28	6.35	99.44		10.45
100	18	2.36	0.58	0.1	0	1.36	0	8.8	0.14	4.54	99.18		-6.038

Table VI: Loss breakdown at AC operation. ($E_1 = 279.6$ V, $E_2 = 124.4$ V, $R = 33.3$ Ω)

Measured loss								
$E_1 + E_2$ [V]	V_{out} (rms) [V]	I_{ac} (rms) [A]	Output power [W]	Loss at DC-DC [W]	Loss at DC-AC [W]	Total loss [W]	DC-DC efficiency [%]	Total efficiency [%]
404	280.2	8.01	2242	5.68	2.86	8.6	99.75	99.62

Calculated loss											Error rate meas. vs calc. [%]
Ideal DC-DC		L	C	Practical DC-half AC		Unfolding inverter			All loss	Total	
Efficiency from DC-DC operation without 50Hz iron loss [%]	Estimated DC-DC loss [W]	Iron loss at 50 Hz [W]	Capacitor loss [W]	Estimated loss + LC loss [W]	Efficiency [%]	Inverter on loss [W]	Line resistance loss [W]	DC-AC total loss [W]	Estimated total loss [W]	efficiency [%]	
99.77	5.157	0.16	0.002	5.32	99.76	1.8	0.64	2.44	7.55	99.65	-9.29

Table VII: Parameters in Table.VI.

inverter line resistance	$r_{invline}$ [mΩ]	10
inverter device resistance	r_{oninv} [mΩ]	14
S_1 case temperature	t_{S1} [°C]	30
S_2 case temperature	t_{S2} [°C]	49
S_3 case temperature	t_{S3} [°C]	43
S_4 case temperature	t_{S4} [°C]	43

Table III indicates that when the output voltage is around 400 V, the error between the measured and estimated calculation is approximately 8% and when the output voltage is 280 V, that error is approximately 15%. See the most right side of the table. The reason of this error can be explained that the error of the direct error measurement inherently has the accuracy problem. The calculated loss has higher accuracy, because measument of current and voltage has higher accuracy in the measurement range. The detail will be discussed in Section 4.4.

Second, the loss breakdown and efficiency of the different DC voltage are shown in Table V when either high side chopper or low side chopper is operated. There are several losses that are not appeared in table III. The upper table V indicates the loss power by the direct measurement. The lower table includes switching loss, switching device conduction loss, PCB line conduction loss, inductor conduction loss, and inductor harmonic iron loss. Those are theoretically and experimentally separated. The iron loss caused by the current ripple and the ripple voltage is calculated based on the measured data in Appendix A. The conduction loss of the devices are assumed to 18 mΩ based on the case temperature as shown in Table IV.

As the results in this table, the right-hand side column indicates that the average error between the measured and calculated ones is 7% and the maximum error is approximately 10%.

4.3 AC output operation and loss estimation including fundamental iron loss of inductor

In table VI, the measured and calculated loss power is compared. The upper table indicates the measured loss and the lower table indicates the measured data based calculated loss power.

Using Fig. 5, the theoretical efficiency (or theoretical loss) under the AC output operation can be calculated, in which the fundamental frequency (50 Hz) inductor iron loss and capacitor loss are not included. Dividing the quarter of one AC cycle into 50 segments, the loss in each segment are integrated, and the total loss can be estimated. The efficiency is obtained as 99.77% as shown in Table VI. This estimated efficiency excludes the inductor 50 Hz iron loss and capacitor 50 Hz loss. These two kinds of are measured and the detail is shown in Appendix A and B. Also the unfolding inverter is assumed to have no switching loss, and the conduction loss at the devices and the line are estimated as shown in Table VII.

As the result of summation of all possible estimation of losses based on measured data, the calculated efficiency becomes 99.65%, while the direct measurement method indicated 99.62%. The difference is very small. The accuracy of the measurement is discussed in the next section.

4.4 Accuracy and the reasonable value of efficiency

The discussion on the accuracy of the efficiency between the measured and calculated in Table VI will be made based on the measurement error of instruments.

(1) First the accuracy is estimated based on the instrument measuring accuracy. Let the measuring error rates of current probe, voltage probe and the power meter in Table II are defined as $A1$, $A2$ and $A3$, which are 0.05%, 0.02% and 0.03%. The power is measured by current and voltage measurements, the estimated power measuring error rate may be calculated as $(1-A1)(1-A2)(1-A3) = 0.1\%$. The output power in Table VI is 2242 [W], thus the possible error becomes 2242×0.1%=2.2 [W]. By the direct measurement approach, the difference of the input and output power is the loss power, thus this value may have 2.2 [W] error. When this error is converted to the efficiency error, it is 2.2/2242=0.1%, and this is literally indicated the efficiency accuracy may be within 0.1%.

(2) On the contrary the ideal DC-AC conversion efficiency 99.77% in the table VI is calculated by the 50 segments averaging of the power and efficiency during a quarter cycle of full rectified waveform in the experiments. This may have maximum error of 10%, because the maximum error rate in table V in the most right-hand side column is 10% as mentioned in section 4.2. The inductor iron loss is estimated by the measurement of current and voltage in Appendix A, thus it may be 0.1% accuracy. The loss of the unfolding inverter is mainly made of the conduction loss. The accuracy of the current probe is 0.05%, however the line resistance 10 mΩ is estimated assuming that it may be similar to the resistance 8 mΩ of PCB line, and it may have a large error. The maximum error rate may be $10/(14\times 2+10) = 0.26$.

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Adding the two kind of maximum error, the total error may be $5.16 \times 0.1 + 2.4 \times 0.26 = 1.14$ [W]. However, this ratio toward the 2242 [W] output is $1.14/2242 = 0.05\%$. As a conclusion the maximum error rate in Table VI is approximately 0.05%.

(3) The discussion here results in the conclusion that the measured efficiency 99.62% in upper Table VI may have 0.1% instrument accuracy, and also the calculate deficiency 99.65% in the lower Table may have 0.05% error in the assumptions. Another measuring approach is under progress, however in this paper the authors conclude that the energy conversion efficiency is 99.6%±0.05 at 2.3 kW output.

5 Conclusions

Concerning the HEECS inverter aimed for a very high efficiency, several improvements were tried since [2], and as a tentative result, the efficiency 99.6% was measured with accuracy of ±0.05%. The detailed loss breakdown methodology was described suitable for the HEECS topology and it is confirmed that the proposed measurement method has reasonable accuracy (0.05%). Further efficiency improvement is expected based on the proposed loss breakdown approach.

Appendix

A: Iron loss estimation based on the measured voltage and current

The iron loss of the inductor is experimentally calculated by drawing the B-H curve. The hysteresis loss of fundamental frequency and also in the ripple frequency is graphically calculated [8]-[11].

Integrating the inductor voltage minus the conduction loss gives the total flux in the inductor, and by plotting the flux - current trajectory in the current - flux plane, the magnetic energy can be calculated [8]. Fig. 6 shows the fundamental frequency flux - current trajectory, which is related to 2242 [W] output power in Table VI. One is the HEECS inverter inductor flux-current trajectory. Another is a case that the same inductor has AC current when 400 Vpeak AC voltage is applied. It is apparent HEECS inverter operation decreases the fundamental iron loss. The HEECS fundamental frequency loss is estimated to be 0.16 [W]. Fig. 7 shows the 20kHz current ripple flux - current trajectories depending on the difference AC instantaneous current. From this graph, iron ripple loss in Table V is obtained. The time delay of the current probe is a key technique for the accurate estimation of the iron loss at high frequency.

B: ESR loss estimation of capacitor

The capacitor current waveform is shown in Fig. 8 which is related to 2242 [W] output in Table VI. From this waveform rms current is calculated and the ems loss is estimated. The film capacitor has 3.5 mΩ as ESR. The ripple current loss at 20 kHz is very small and it is neglected.

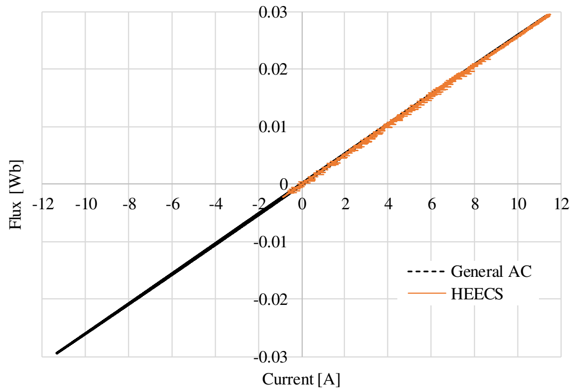

Fig. 6: Flux - current trajectory of inductor used in 2 type inverter at fundamental frequency.

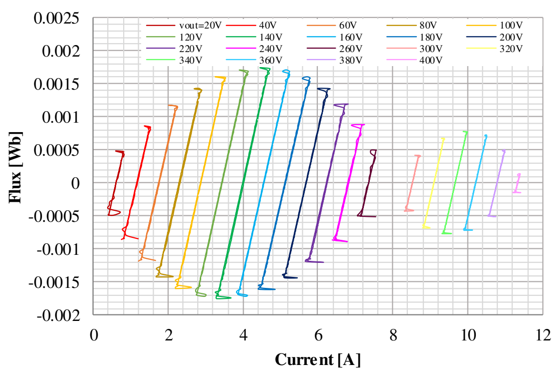

Fig. 7: Flux - current trajectory of inductor used in HEECS inverter at carrier frequency.

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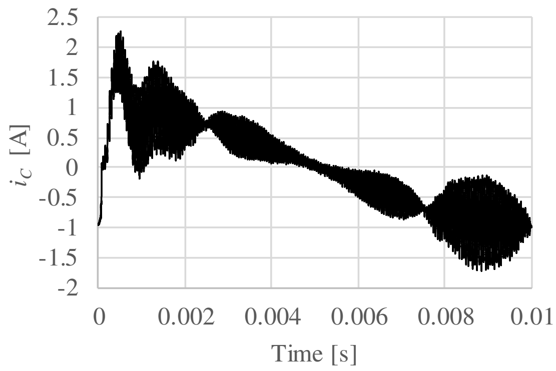

Fig. 8: Capacitor current in an half-sinusoidal operation. ($E_1 = 279.6$ V, $E_2 = 124.4$ V, $R = 33.3\ \Omega$, $L = 2.43$ mH, $C = 8\ \mu$F, 400 Vpeak AC output voltage)

Acknowledgments

Authors express their sincere thanks for the Mr. Tanaka and Kobayashi who is belonging to RITA Electronics, Ltd. to provide a technical support in estimating PCB resistance estimation. This work was supported in part by JSPS KAKENHI Grant Number 17H06147.

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